EE 330

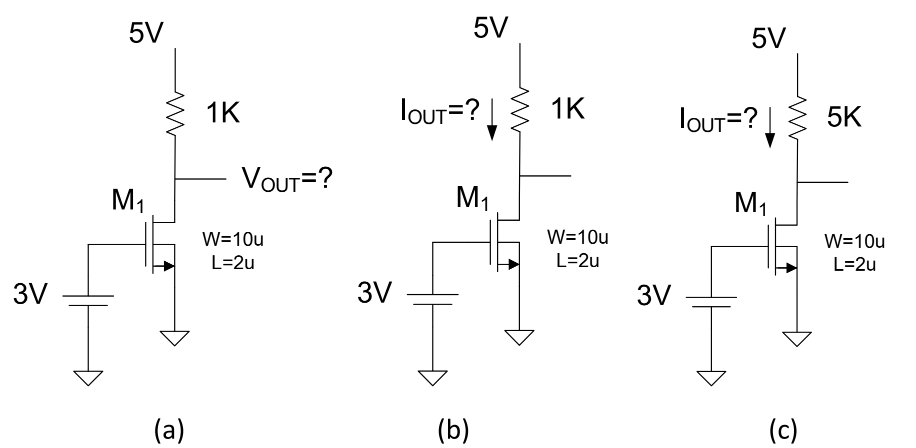
Homework 7 Spring 2024

Due Friday, March 1 at 12:00 noon

Unless stated to the contrary, assume all MOS transistors have model parameters $\mu_n C_{OX}=100\mu A/V^2$, $V_{Tn}=0.75V$, $\mu_n/\mu_p=3$, $V_{Tp}=-0.75V$, $C_{OX}=4fF/\mu^2$, $\lambda=0, \gamma=0$ and all BJT transistors have model parameters $J_S A= 10^{-12}$ A, $\beta_n=100$, and $\beta_p=30$. If any other parameters are needed, consult the parameter list appended to this assignment.

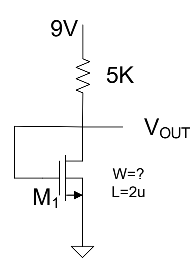
Problem 1

Analytically determine the quantities indicated with a "?".



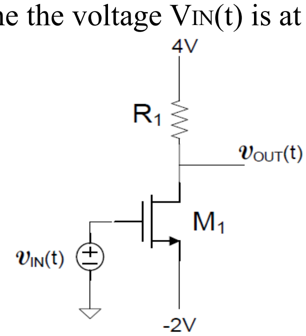
Problem 2

Determine W so that V_{OUT} = 6V

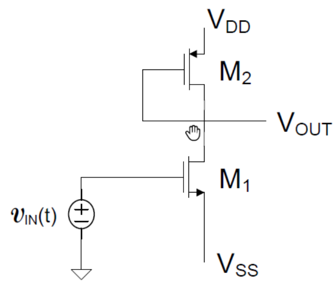


Problem 3

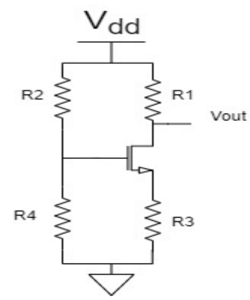
Determine the maximum value of R_1 that will keep M_1 in saturation. M_1 has dimensions $W=12\mu$ and $L=2\mu$. Assume the voltage $V_{IN}(t)$ is at 0 V DC.



Problem 4 Consider the following circuit. Determine the output voltage if V_{DD}=3V, V_{SS}=-2V, W_1=8µ, L_1=2µ, W_2=50µ and L_2=2µ. Assume the magnitude of the input is arbitrarily small.

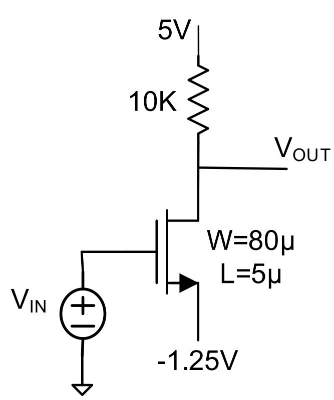


Problem 5 Find V_{OUT} for V_{DD}=10V, R_1=5K, R_2=10K, R_3=2K, R_4=90K assuming the transistor is minimum sized in a process that uses the same design rules as the ON 0.5µ CMOS process that has been used in laboratory experiments.

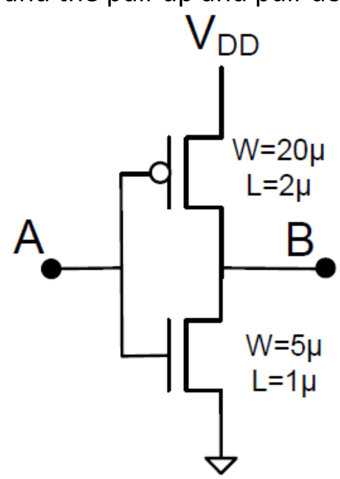


Problem 6 Consider the following circuit (remember to use the model parameters given at the top of this assignment).

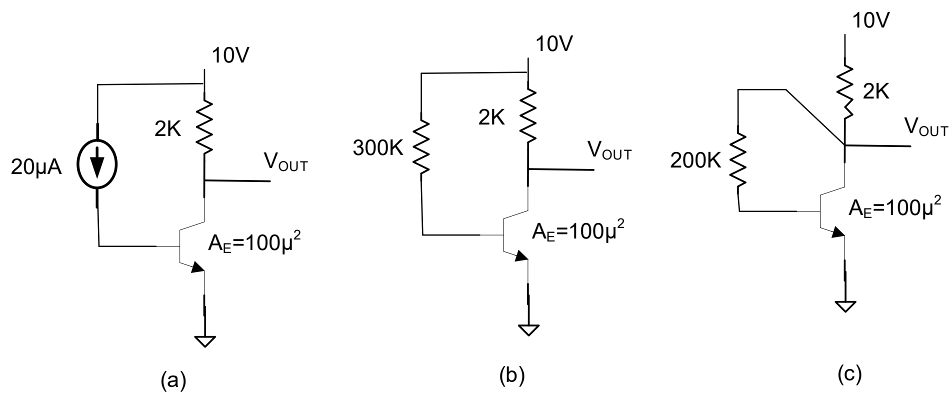
a) Determine V_{OUT} if V_{IN}=0V
b) If V_{IN} is a square waveform going between 0V and 0.1V, the output will also be a square wave. Determine the output waveform for this small square wave input.
c) This circuit serves as an amplifier and the gain can be defined to be the ratio between the peak-to-peak value of the output to that of the input. What is the gain of this amplifier with the 0.1V p-p square waveform at the input?



Problem 7 Consider the following inverter. Determine the switch-level model for this inverter that includes the input capacitance and the pull-up and pull-down resistors if V_{DD}=3.5V..



Problem 8 Determine the output voltage for the following circuits.



Problem 9 & 10 Implement an 8 to 3 encoder and 3 to 8 decoder, both with an active low enable pin, using Verilog. When the encoder/decoder is disabled, its output should be low. Design a testbench proving function using Verilog. Submit module code, testbench code, and Modelsim waveforms.

Passive Process Parameters for CMOS Process											
	N+	P+	POLY	POLY2	HR_P2	M1	M2	M3	N/PLY	N_W	UNITS

RESISTANCES											
Sheet Resistance	84	105	23.5	999	44	0.09	0.10	0.05	825	815	Ohms/sq
Contact Resistance	65	150	17		29		0.97	0.79			Ohms
CAPACITANCES											
Area (substrate)	425	731	84			27	12	7		37	af/µm^2
Area (N+ active)			2434			35	16	11			af/µm^2
Area (P+active)			2335								af/µm^2
Area (POLY)				938		56	15	9			af/µm^2
Area (POLY2)						49					af/µm^2
Area (metal 1)							31	13			af/µm^2
Area (metal 2)								35			af/µm^2
Fringe (substrate)	344	238				49	33	23			af/µm
Fringe (poly)						59	38	28			af/µm
Fringe (metal 1)							51	34			af/µm
Fringe (metal 2)								52			af/µm
Overlap (N+active)			232								af/µm
Overlap (P+active)			312								af/µm